FPGA Implementation of Flood Monitoring System

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Abstract—Flood is one of huge disaster in India which affects human, fertile agricultural land, soil, animals etc. It is not possible to full control flood but we can definitely reduce damage done by flood & its impact on human & animal life. This paper explains flood prediction system using the sensor and processing in the FPGA board. Sensor is used to measure the real world parameters like water level, water pressure, temperature, flow etc. Output of the sensor is then given to the FPGA board to convert physical data to digital data to do the further processing on board. This system is implemented in river in such way that sensor will be able to detect water level at any time. Predicting flood before its actual occurrence can buy the sufficient time for residents to evacuate the nearby areas, preventing the loss of life and the property. Design has been prototyped on the Xilinx Spartan 3E FPGA starter kit board.

Keywords—FPGA, Spartan 3E

I. INTRODUCTION

Flooding is one of the key disasters occurring in different region of the world. Flood has been one of the major problems in most of the states in India. Flooding happens after intense rains, when rivers overflow, when oceanic waves come back onto land, when snow melts fast or onedams overflow or break. Flooding is that the most typical of all natural hazards in Asian nation particularly throughout monsoon and causes important and irrecoverable harm to life and properties of the people. Although, we may be able to predict rainfall or track rainstorm accurately via satellite images, we have to have real-time monitored information like flow, rainfall level, or water level etc. So that sensible action can be taken before hand to prevent flooding.

In Orissa, flooding is a recurrent event affecting the entire state, especially the river bank and coastal areas. Every year, it causes the lives and damages to the infrastructure, agricultural production and the severely affects the local economic development. As a result of this, flood management of state is a crucial challenge. Disaster flood alert system using pressure sensors is one of the cheapest technology available today which is useful to make the people alert from disaster flood. In this project pressure sensors are used to find out the water level of the river/dam.

Every year disaster flood has its adverse effects. Due to this government have to face more critical problems. Many people with animals have to strive for their life. Overall it affects the ecological balance, crops dories due to excess water and is carried away with it. Soil erosion takes place to large extent. Flood monitoring using real-time sensor is one of non-structural flood control measures.

Losses due to the flooding can be reduced by means of the measures such as forecasting, monitoring, simulation, analysis and evaluation. The effective implementation of the flood monitoring and the warning system is the non-trivial, since it requires the reliability coupled with availability of related information.

II. SYSTEM DESIGN

The system architecture of the system design is given in figure 1. The flood parameters like water pressure, water level, flow etc. are measured by the sensor. The output voltage from the sensor is given to the onboard ADC present on the Spartan 3E
FPGA board and display data on the Android phone using Bluetooth.

Fig1. Proposed block diagram of system

III. MODULE DESIGN

The different components or block of the system design are:-

A. SENSORS:

1. FLOW SENSOR
   This sensor is used to measure flow rate of water in a river. It is used to measure depth/level of liquid in a container. As the water rises and reaches level of float switch, it begins to float which is going from vertical to horizontal. When the float sensor exceed the set point value and microcontroller continuously scans for float and float sensor will sense the particular parameter, these parameters are in millivolts (0-1v), then analog to digital converter converts these parameters i.e analog voltage (given by the float sensor) into digital signal. This digital signal is then given to FPGA for further processing.

2. WATER LEVEL SENSOR
   Water level is measured in three different level by this sensor. Water level sensor is typically used to measure the depth/level of liquid in a container. As the water rises and reaches the level of the different electrode, it begins to level going from vertical to horizontal. When the level sensor values exceed the set point and the microcontroller continuously scans for the level and level sensor will sense the particular parameter. These parameters are in millivolts (0-1v), then ADC converts these parameters into digital form. This digital signal is then given to FPGA for further processing.

3. RAINFALL SENSOR
   Using rainfall sensor we are measuring rainfall in mm. Rainfall sensor is used to measure rainfall within that area in mm. Funnel is used to collect rainfall & further connected to measuring system.

B. PRE-AMPLIFIER & ADC INTERFACING:
   Preamplifier amplify the analog output of sensor to desire level so that can be applied to ADC, where ADC converts the signal in digital form. FPGA and pre-amplifier are interfaced with the help of various signals. Serial Peripheral Interface bus is used for communication between pre-amplifier and the FPGA. SPI bus is also shared between ADC, DAC, Platform Flash and Strata Flash. So when one device is interfacing with SPI bus other device should be disable to enable proper interface between the on-going connection. SPI signals which control proper connection of pre-amplifier and FPGA are:
   - **SPI_MOSI**: It is an internal bus with pin T4 on the FPGA board. It is the output signal to amplifier. This bus gives serial data. It gives programmable gain byte.
   - **AMP_CS**: SPI bus with pin N7 on the FPGA board. Directed from FPGA to amplifier. Active-low chip select signal. When the signal returns high the amplifier gain is set.
   - **SPI_SCK**: Pin U16 on the FPGA board. Directed from FPGA to amplifier. Clock signal which sets the gain.
• **AMP_SHDN**: Pin P7 on FPGA board. FPGA to the amplifier.
• **AMP_DOUT**: Pin E18 on the FPGA board. Directed from AMP to FPGA. Echoes earlier AMP gain data back to FPGA.

![Fig3. SPI Serial interfacing to amplifier](image)

**C. BLUETOOTH INTERFACING:**
Bluetooth is used to connect FPGA system with application on android phone to show the data. Bluetooth is the wireless standard technology used for exchanging the data over short distances (using the short-wavelength UHF radio waves in ISM band from 2.4 to 2.485 GHz) from the fixed and mobile devices and building the personal area networks (PANs). Invented by the telecom vendor Ericsson in the 1994, it was originally conceived as the wireless alternative to the RS-232 data cables. It can used to connect several devices and overcoming problems of synchronization.

Android platform includes support for Bluetooth network stack, which allows the devices to wirelessly exchange the data with any other Bluetooth devices. The application framework provides access to Bluetooth functionality through Android Bluetooth APIs. These APIs connect applications wirelessly to the other Bluetooth devices, which enabling point-to-point and the multipoint wireless features.

Using Bluetooth APIs, an Android application can perform the following:
- Scan for the other Bluetooth devices
- Query local Bluetooth adapter for paired Bluetooth devices
- Establish RFCOMM channels
- Connect to other device through service discovery
- Transfer the data to and from other devices
- Manage multiple connections

**D. LCD INTERFACING:**
The data from sensors is also displayed on 16 x 2 LCD display.

The Spartan-3E FPGA board includes 2-line of 16-character LCD. 4-bit data interface method is used by FPGA to control the LCD. This LCD display also support 8-bit data interfacing, but still the FPGA board use only 4-bit data interface so that it can minimize the total pin count and also be compatible with other Xilinx development board. Every byte of the command provided to the LCD interfacing occurs using 4 bit interfacing hence each command is get divided into the two 4 bit transmissions spaced by 1us. Successive commands (all sequential 4 bit transmission) need to be separate from next for 40us. The 3 major processes in interfacing the LCD are initialization of 4 bit interfacing; the second is to set commands for displaying operation and 3rd is writing of character. One design machine is for power on initialization process, one state machine is for transmitting commands and data byte to LCD module and the other one is to commence the power on initialization process.

**E. DC MOTOR INTERFACING:**
The gates of dam can be controlled using DC MOTOR. DC motors were used to drive the application physically as per the requirement provided by the software. The dc motor works on the 12v.

To drive the dc motor, we need motor driver called L293D IC. This motor driver is capable of driving two dc motors simultaneously. To protect the dc motor from the back EMF generated by dc motor while changing direction of rotation, motor driver have internal protection suit. We can also provide back EMF protection suit by connecting four diode configurations across each dc motor.

**F. FPGA KIT:**
A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence “field-programmable”. The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC). Some FPGAs have analog features with digital functions. Most used analog feature is programmable drive strength and slew rate on each output pin, allowing
engineers to set the slew rates on the lightly loaded pins that would otherwise ring unacceptably, and to set the stronger, faster rates on heavily loaded pins on the high-speed channels that may run too slowly. Another common analog feature is differential comparators on i/p pins designed to be connected to the differential signalling channels. A few mixed signal FPGAs have the integrated peripheral ADCs and DACs with the analog signal conditioning blocks allowing them to operate as system-on-a-chip. Such devices blur line between FPGA, which carries digital 1s and 0s on its field-programmable analog array (FPAA) and internal programmable interconnect fabric, which carries the analog values on its internal programmable interconnect fabric.

IV. CONCLUSION
In this project embedded system on flood monitoring is designed and implemented in hardware on Spartan-3E Starter Kit FPGA board. The system is implemented and tested in the laboratory. The output result is obtained in Hyper Terminal window and also display on the LCD. This design can be of great help in real life in the flood prone area especially near the river and dam.

V. REFERANCE